FIG. 1
(PRIOR ART)

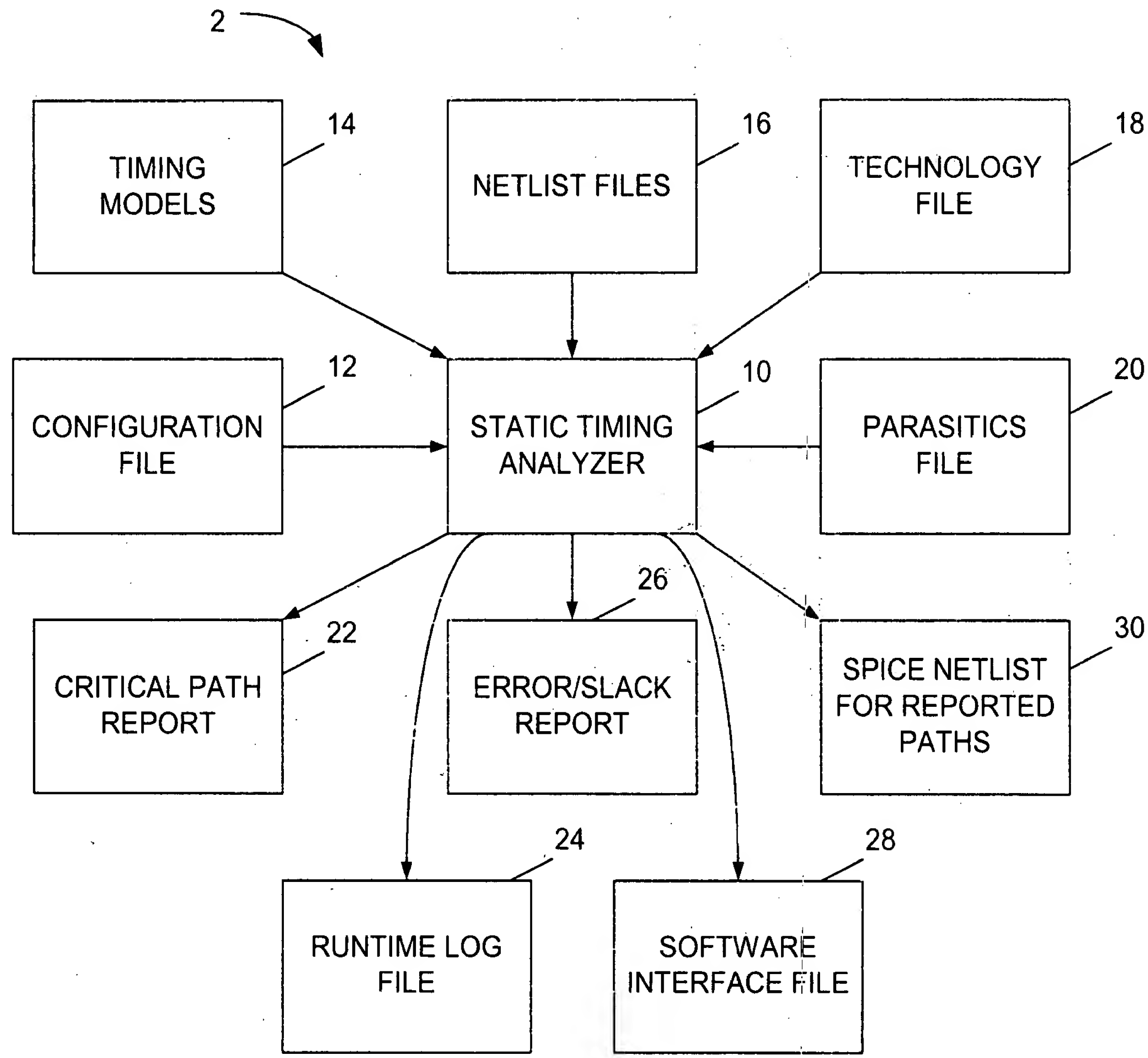


FIG. 2

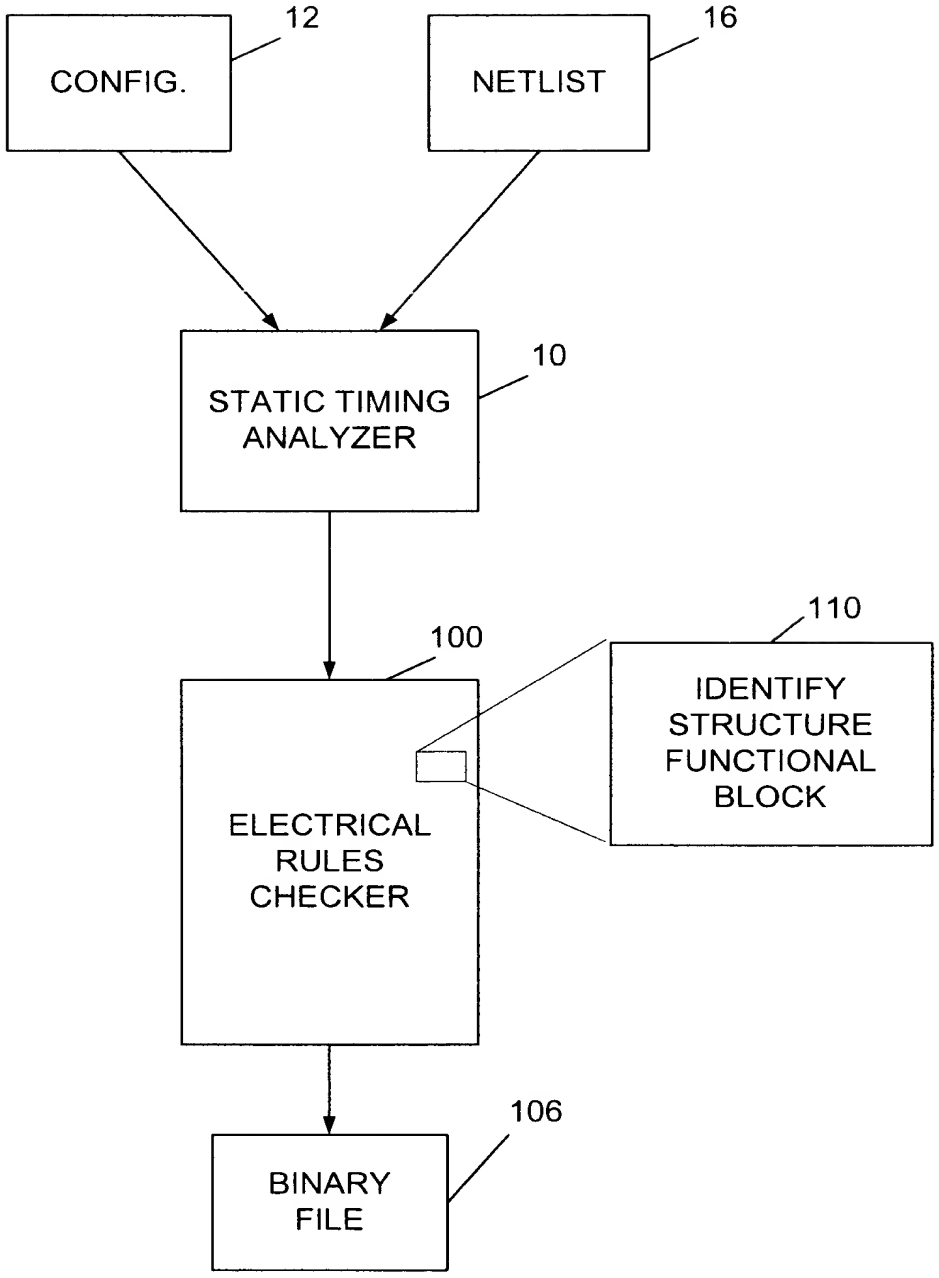

CONFIG.
12
NETLIST
16
STATIC TIMING ANALYZER
10
100
110
IDENTIFY STRUCTURE FUNCTIONAL BLOCK
ELECTRICAL RULES CHECKER
106
BINARY FILE

FIG. 3

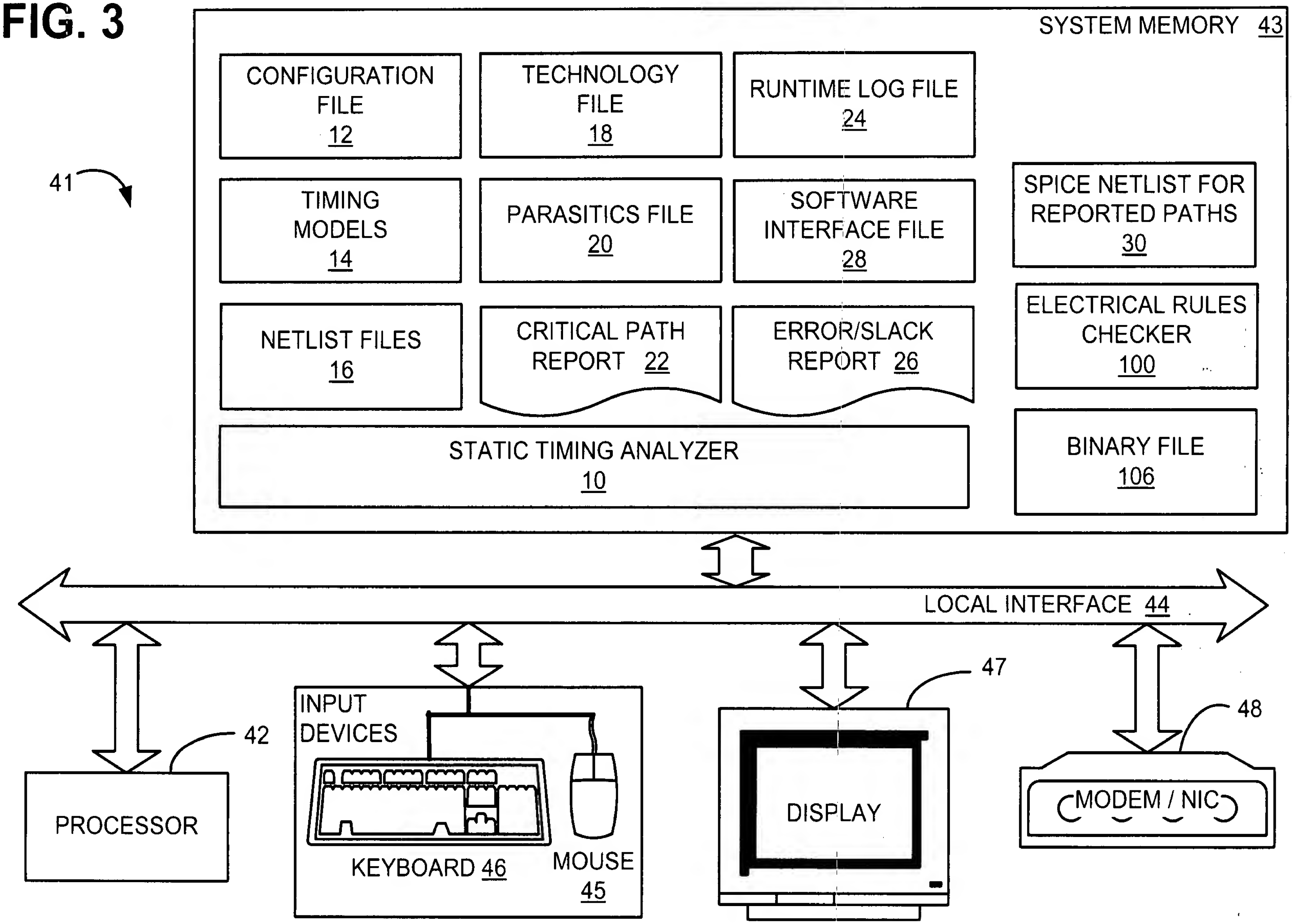

41
SYSTEM MEMORY 43
CONFIGURATION FILE 12
TECHNOLOGY FILE 18
RUNTIME LOG FILE 24
TIMING MODELS 14
PARASITICS FILE 20
SOFTWARE INTERFACE FILE 28
SPICE NETLIST FOR REPORTED PATHS 30
NETLIST FILES 16
CRITICAL PATH REPORT 22
ERROR/SLACK REPORT 26
ELECTRICAL RULES CHECKER 100
STATIC TIMING ANALYZER 10
BINARY FILE 106
LOCAL INTERFACE 44
42
PROCESSOR
INPUT DEVICES
KEYBOARD 46
MOUSE 45
47
DISPLAY
48
MODEM / NIC

FIG. 4A

ELEMENT {~~~~
~~~~
Complementary Pass FET
Special Complementary Pass FET
RAM Cells
Single Pass FET
Feedback FET
Static Gates
Probable
~~~~~
~~~~~
Direction: Unset, Bidirectional, Source-to-Drain, Drain-to-Source,
~~~~~}

# FIG. 4B

NODE {~~~~
~~~~
Output
Inverter Outputs
Latch
Precharged
Dynamic
Static
Clock driver
Mux Output
~~~~~
~~~~~}
~~~~~

FIG. 5A

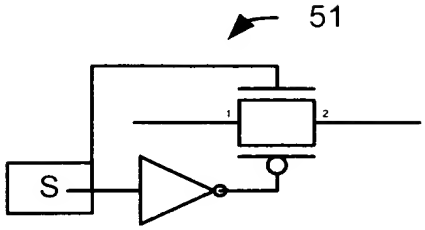


FIG. 5B

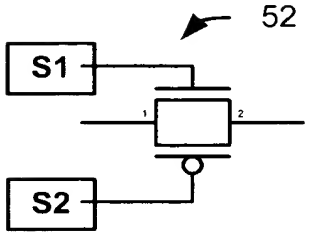


FIG. 5C

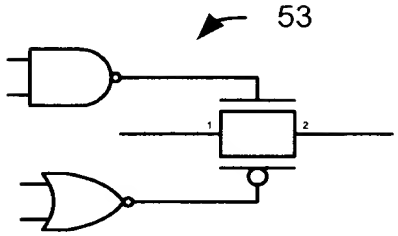


FIG. 6A

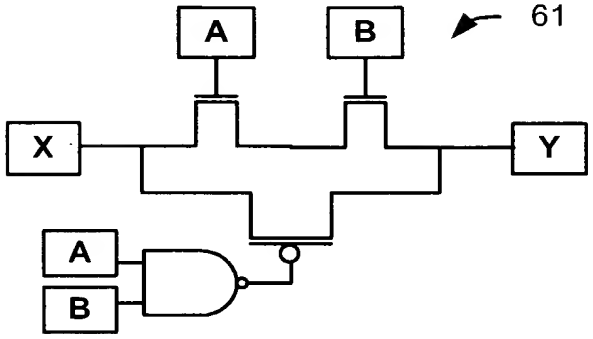


FIG. 6B

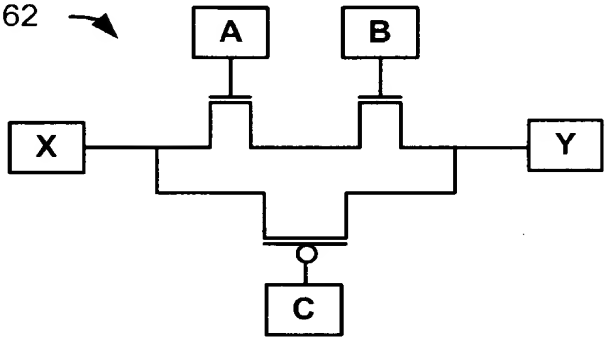


FIG. 7A

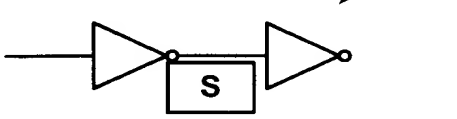


FIG. 7B

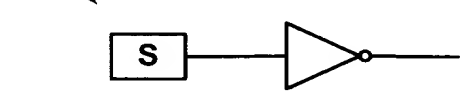


FIG. 8A

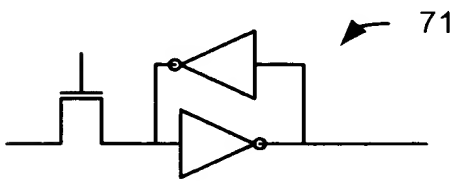
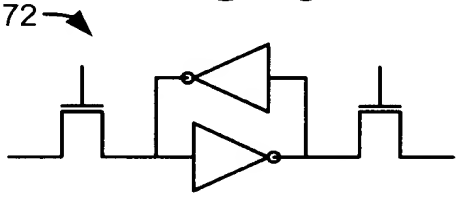


FIG. 8B



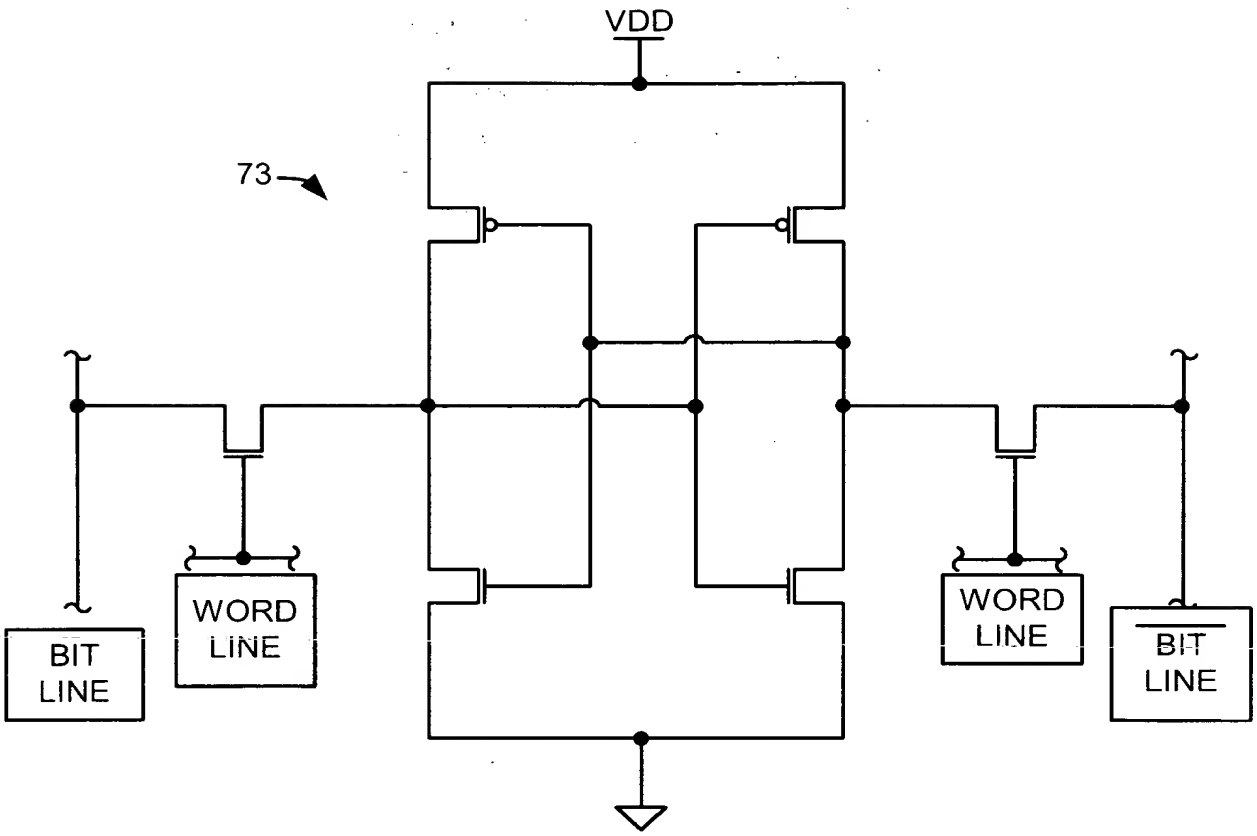


FIG. 9

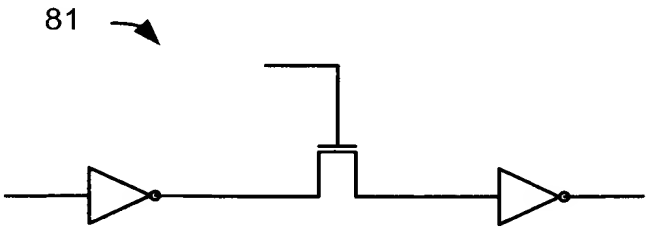


FIG. 10A

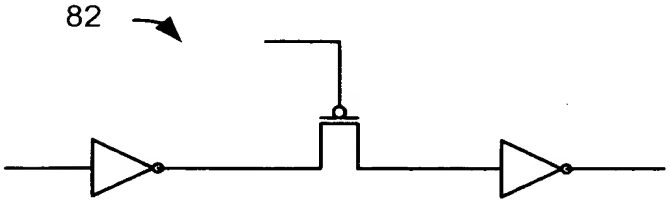


FIG. 10B

FIG. 11

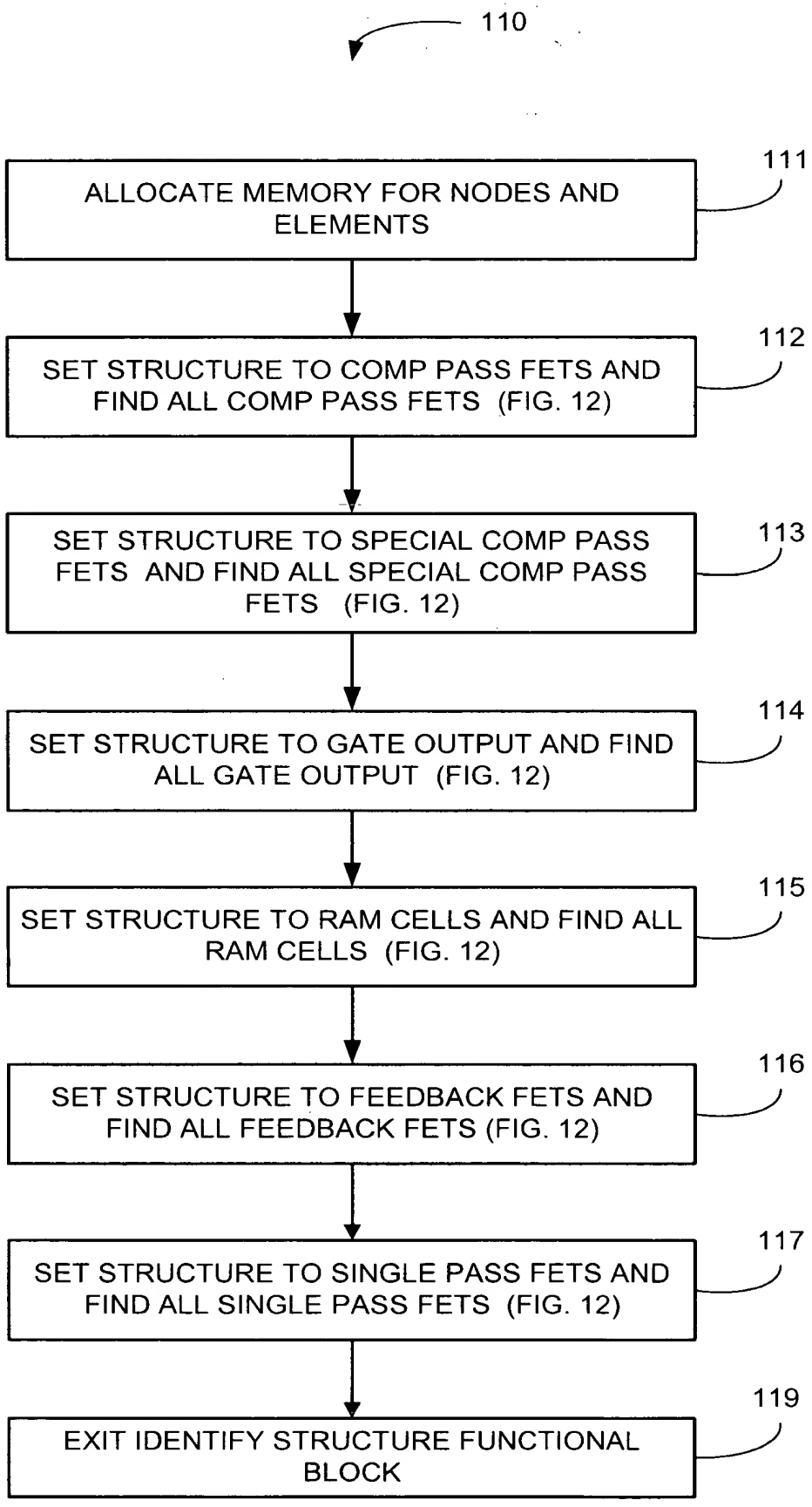
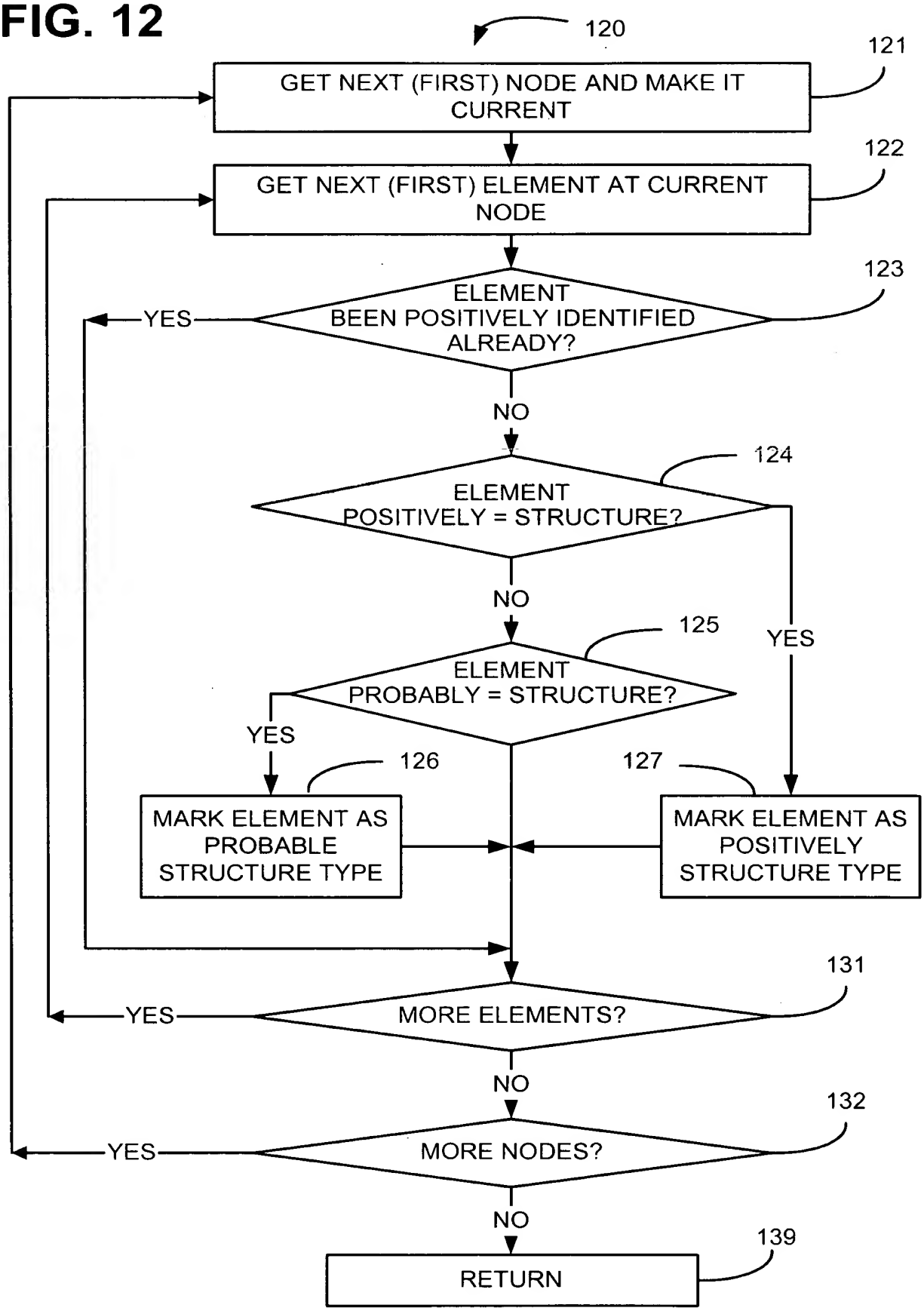

110
ALLOCATE MEMORY FOR NODES AND ELEMENTS
111
SET STRUCTURE TO COMP PASS FETS AND FIND ALL COMP PASS FETS (FIG. 12)
112
SET STRUCTURE TO SPECIAL COMP PASS FETS AND FIND ALL SPECIAL COMP PASS FETS (FIG. 12)
113
SET STRUCTURE TO GATE OUTPUT AND FIND ALL GATE OUTPUT (FIG. 12)
114
SET STRUCTURE TO RAM CELLS AND FIND ALL RAM CELLS (FIG. 12)
115
SET STRUCTURE TO FEEDBACK FETS AND FIND ALL FEEDBACK FETS (FIG. 12)
116
SET STRUCTURE TO SINGLE PASS FETS AND FIND ALL SINGLE PASS FETS (FIG. 12)
117
EXIT IDENTIFY STRUCTURE FUNCTIONAL BLOCK
119

FIG. 12


120
121
GET NEXT (FIRST) NODE AND MAKE IT CURRENT
122
GET NEXT (FIRST) ELEMENT AT CURRENT NODE
123
ELEMENT BEEN POSITIVELY IDENTIFIED ALREADY?
YES
NO
124
ELEMENT POSITIVELY = STRUCTURE?
NO
YES
125
ELEMENT PROBABLY = STRUCTURE?
YES
126
MARK ELEMENT AS PROBABLE STRUCTURE TYPE
127
MARK ELEMENT AS POSITIVELY STRUCTURE TYPE
131
MORE ELEMENTS?
YES
NO
132
MORE NODES?
YES
NO
139
RETURN